

We claim:

1. A noise suppression method, comprising:
generating a frequency signal from a PLL based on a reference signal; and
removing noise from the frequency signal by shifting a spurious signal of a predetermined order outside a loop bandwidth of the PLL.
2. The method of claim 1, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter in the PLL.
3. The method of claim 1, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of a loop filter in the PLL.
4. The method of claim 1, wherein said noise is removed by:
shifting a first-order spurious signal outside the loop bandwidth of the PLL.
5. The method of claim 1, further comprising:
setting a frequency divider in a feedback loop of the PLL to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

6. The method of claim 5, wherein the frequency divider is set by a Sigma-Delta modulator.

7. The method of claim 6, wherein the frequency divider is a pulse swallow frequency divider.

8. The method of claim 7, further comprising:
computing a modulation ratio of the Sigma-Delta modulator based on the loop bandwidth of the PLL; and
setting the value of the pulse swallow frequency divider based on the modulation ratio computed for the Sigma-Delta modulator.

9. The method of claim 8, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

10. The method of claim 9, wherein the frequency signal of the PLL (f_{vco}) is generated in accordance with the following equation: $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$.

11. The method of claim 9, further comprising:

modulating the reference signal input into the PLL.

12. The method of claim 11, wherein the frequency signal of the PLL (f_{vco}) is generated

in accordance with the following equation: $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left(\frac{N_{mod}}{D_{mod}} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$,

where f_{ref} is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P_{new} is the value of the program counter, S_{new} is the value of the swallow counter, N_{new} and D_{new} is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

13. The method of claim 11, further comprising:

using the modulated reference signal as a comparison signal for the PLL as long as harmonics of the modulated reference signal and the unmodulated reference signal are not coincident.

14. The method of claim 1, wherein the spurious signal is generated by a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

15. A method for suppressing noise in a frequency generator, comprising:
modulating a reference signal; and
generating a frequency signal from a PLL based on the modulated reference signal,
wherein modulating the reference frequency generates a frequency separation between harmonics of
the modulated reference signal and the reference signal that suppresses noise in the frequency signal.

16. The method of claim 15, further comprising:
using the modulated reference signal to generate the frequency signal from the PLL
as long as the harmonics of the modulated reference signal is not coincident with the harmonics of the
reference signal.

17. A frequency generator, comprising:
a phase-locked loop which generates a frequency signal based on a reference signal;
and
a noise suppressor which shifts a spurious signal of a predetermined order outside a
loop bandwidth of the PLL.

18. The frequency generator of claim 17, wherein the phase-locked loop includes a loop
filter, and the loop bandwidth is defined by a cutoff frequency of the loop filter.

19. The frequency generator of claim 17, wherein the phase-locked loop includes a loop filter, and the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of the loop filter.

20. The frequency generator of claim 17, wherein the noise suppressor shifts a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

21. The frequency generator of claim 17, wherein the noise suppressor includes:
a frequency divider in a feedback loop of the phase-locked loop; and
a controller which sets the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

22. The frequency generator of claim 21, wherein the controller includes a Sigma-Delta modulator.

23. The frequency generator of claim 22, wherein the frequency divider is a pulse swallow frequency divider.

24. The frequency generator of claim 23, wherein the pulse swallow frequency divider is set to said value based on a modulation ratio of the Sigma-Delta modulator.

25. The frequency generator of claim 24, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

26. The method of claim 25, wherein the PLL generates the frequency signal (f_{vco}) in accordance with the following equation: $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$.

27. The frequency generator of claim 25, further comprising:
a modulator which modulates the reference signal input into the phase-locked loop.

28. The frequency generator of claim 27, wherein the PLL generates the frequency signal in accordance with the following equation: $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left(\frac{N_{mod}}{D_{mod}} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$,

where f_{ref} is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P_{new} is the value of the program counter, S_{new} is the value of the swallow counter, N_{new} and D_{new} is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

29. The frequency generator of claim 27, wherein the modulated reference signal is used as a comparison signal for the PLL as long as harmonics of the modulated reference signal are not coincident with harmonics of the unmodulated reference signal.

30. The frequency generator of claim 17, wherein the spurious signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

31. A frequency generator, comprising:
a modulator which modulates a reference signal; and
a PLL which generates a frequency signal based on the modulated reference signal,
said modulator generating a frequency separation between harmonics of the modulated reference signal and the reference signal that suppresses noise in the frequency signal.

32. The frequency generator of claim 31, wherein the PLL generates the frequency signal using the modulated reference signal as long as the harmonics of the modulated reference signal are not coincident with the harmonics of the reference signal.

33. A system for controlling a PLL, comprising:
a divider which divides a frequency signal output from the PLL; and
a controller which sets the divider to a value which shifts a spurious noise signal of a predetermined order outside loop bandwidth of the PLL.

34. The system of claim 33, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter of the PLL.

35. The system of claim 33, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal and a cutoff frequency of a loop filter in the PLL.

36. The system of claim 33, the controller shifts a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

37. The system of claim 33, wherein the divider is a pulse swallow frequency divider and the controller includes a Sigma-Delta modulator.

38. The system of claim 37, wherein the Sigma-Delta modulator sets the value of the pulse swallow frequency divider based on a modulation ratio of the Sigma-Delta modulator.

39. The system of claim 38, wherein the pulse swallow frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

40. The system of claim 39, wherein the controller controls the PLL to generate the output

frequency signal in accordance with the equation $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left(\frac{N_{mod}}{D_{mod}} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$.

41. The system of claim 39, wherein the controller includes:

a modulator which modulates a reference signal of the PLL.

42. The system of claim 41, wherein the controller controls the PLL to generate the output

frequency signal based on the equation $f_{vco} = \left(\frac{f_{ref}}{R} \right) \left(\frac{N_{mod}}{D_{mod}} \right) \left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}} \right) \right)$, where f_{ref}

is the reference signal, R is a value of a reference signal divider, N_{mod} and D_{mod} define a modulation ratio for the reference signal, P_{new} is the value of the program counter, S_{new} is the value of the swallow counter, N_{new} and D_{new} is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

43. The system of claim 41, wherein the modulated reference signal is used as a comparison signal of the PLL as long as a harmonic of the modulated reference signal is not coincident with a harmonic of unmodulated reference signal.

44. The system of claim 33, wherein the spurious noise signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.